

## Characterizing the Two-Dimensional Doping Concentration inside Silicon Nanowires Using Scanning Spreading Resistance Microscopy

Thomas Hantschel<sup>1</sup>, Volker Schulz<sup>1</sup>, Andreas Schulze<sup>1,3</sup>, Esteban Angeletti<sup>1</sup>, Firat Guder<sup>1</sup>, Volker Schmidt<sup>2</sup>, Stephan Senz<sup>2</sup>, Pierre Eyben<sup>1</sup> and Wilfried Vandervorst<sup>1,3</sup>

<sup>1</sup>IMEC, Kapeldreef 75, B-3001 Leuven, Belgium.

<sup>2</sup>Max Planck Institute of Microstructure Physics, Weinberg 2, D-06120 Halle, Germany.

<sup>3</sup>Instituut voor Kern- en Stralingsfysica, K. U. Leuven, Celestijnenlaan 200D, B-3001 Leuven, Belgium.

### ABSTRACT

The characterization of doped regions inside silicon nanowire structures poses a challenge which must be overcome if these structures are to be incorporated into future electronic devices. Precise cross-sectioning of the nanowire along its longitudinal axis is required, followed by two-dimensional electrical measurements with nanometer spatial resolution. The authors have developed an approach to cross-section silicon nanowires and to characterize them by scanning spreading resistance microscopy (SSRM). This paper describes a cleaving- and polishing-based cross-sectioning method for silicon nanowires. High resolution SSRM measurements are demonstrated for epitaxially grown and etched silicon nanowires.

### INTRODUCTION

Silicon nanowires are candidates as building blocks for future integrated devices such as tunnel field-effect transistors (TFET)[1]. Various fabrication schemes for silicon nanowires have already been demonstrated [2-5]. The precise control of the nanowire doping, however, is still a big challenge as one has not been able yet to characterize doped regions directly inside nanowires. The characterization requires two-dimensional electrical measurements on the cross-section of the nanowire. The method of choice for characterizing the doped regions of state-of-the-art silicon devices is scanning spreading resistance microscopy (SSRM) [6,7]. In SSRM, a sharp diamond tip is scanned over the device cross-section measuring the local spreading resistance which is linked to the carrier concentration. A spatial resolution below 1 nm has been demonstrated. The application of SSRM for silicon nanowire analysis is thus highly desired. However, it is common in SSRM to use long transistor test structures in the order of tenths to hundreds of micrometers which facilitates the cross-sectioning, an approach which cannot be applied to silicon nanowires of fixed diameter and confined volume. Therefore, we have developed both a cleaving- and polishing-based procedure for cross-sectioning silicon nanowires and applied these procedures to etched and to epitaxially grown silicon nanowires. Our SSRM measurements illustrate that two-dimensional electrical images of silicon nanowires can be obtained with high spatial resolution. This paper explains the developed approach and applies it to different nanowire samples.

### EXPERIMENTAL DETAILS

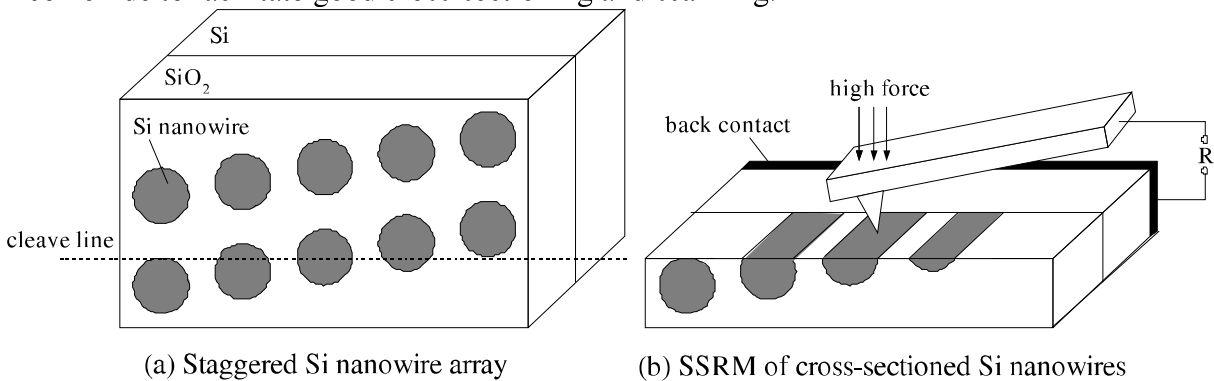
The nanowire samples are scribed with a manual scriber tool with optical microscope from Karl Suss of model RA120 and are cleaved afterwards by using glass cutter pliers from

Fletcher Terry of model gold tip. For nanowire polishing, first a microscope glass slide or a silicon chip is glued against the sample surface using M-Bond 610 at 150°C for 30 min. A sequence of polishing steps is then carried out using a Mecapol P200 tool from Presi using diamond papers whereby the grain size is gradually reduced from 15 to 0.1 μm. It is followed by polishing steps with Al<sub>2</sub>O<sub>3</sub> lapping films with decreasing grain sizes of 1 to 0.05 μm. The sample is rinsed in deionized water and dried by nitrogen blowing after each polishing step.

The inspection of the nanowire cross-section and marking of the nanowire region to be measured is carried out in a nanoprobing system consisting of an FEI XL30 scanning electron microscope (SEM), a Kleindiek 4-point probing unit and a Keithley 4200 parameter analyzer. The SSRM measurements are done in a Veeco Dimension 3100 atomic force microscope (AFM) with attached SSRM application module. A bias voltage of 500 mV is used. The SSRM probes are in-house fabricated nickel cantilevers with integrated boron-doped diamond tips with sub-nanometer electrical resolution [8,9].

## CROSS-SECTIONING OF SILICON NANOWIRES

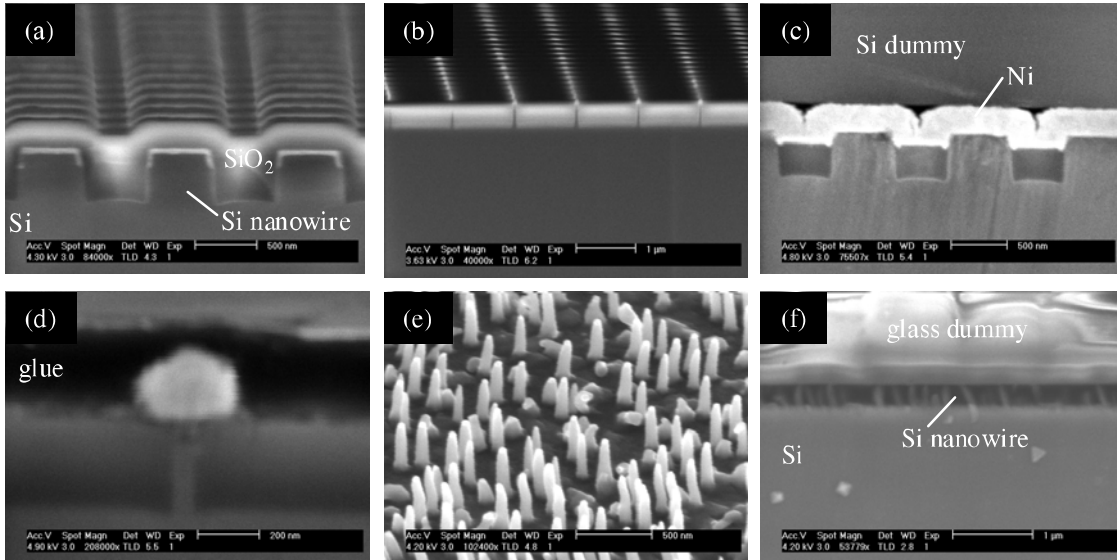
Figure 1 shows the basic scheme for preparing Si nanowires for SSRM measurements which have been etched or grown on top of Si wafers in a regular pattern for SSRM measurements. The proper cross-sectioning of the Si nanowires with typical root-mean-square (RMS) values of  $\leq 0.2$  nm is the key for high-resolution measurements. Ideally, nanowires of the same diameter are placed into an array whereby staggering them perpendicular to the sectioning direction (figure 1a). The staggering distance should be one fourth to one tenth of the nanowire diameter to ensure that there are always a few nanowire cross-sections available along the sectioning line. It is preferred that the nanowires are embedded into a supporting material such as silicon oxide to facilitate good cross-sectioning and scanning.



**Figure 1.** Concept of SSRM measurements on Si nanowires: a staggered nanowire layout facilitates the nanowire cleaving (a); a conductive diamond tip scans the cross-section of the Si nanowire while measuring the local spreading resistance (b).

The nanowires are cleaved by putting first a 1-2 mm long scribe mark parallel or perpendicular to the (100)-wafer flat at the desired cleaving location. For obtaining a good cleaving quality, it is required that the scribe is put about 5 mm away from the array of nanowires as the first few millimeters of the cleavage are of poor quality. Although cleaving is preferred because of lower surface roughness and ease of procedure, additional nanowire polishing is done when metal contact layers are involved (metal films do not cleave well). Figures 2a and 2b show cross-sectioned silicon nanowires prepared by cleaving with diameters

of 500 and 50 nm. The advantage of a staggered design is illustrated in figure 2b where four nanowire cross-sections are available for SSRM measurements before the cleavage runs out of the nanowires. Figures 2c and 2d are examples for polished nanowire cross-sections with electroplated nickel caps on top. The cross-section of the 40 nm diameter nanowire demonstrates that the developed procedures allow also for sub-50 nm structures with thick metal layers.

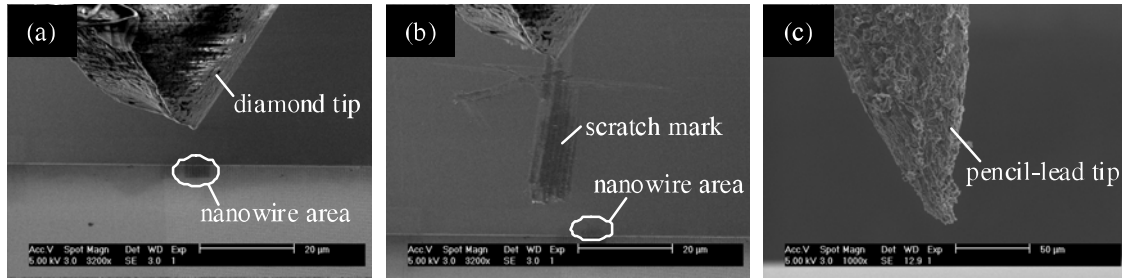


**Figure 2.** Cross-sectioning of Si nanowires: Staggered Si nanowires embedded into  $\text{SiO}_2$  with 500 nm (a) and 50 nm diameter (b) prepared by cleaving; Si nanowires of 500 nm (c) and 40 nm (d) diameter with Ni cap prepared by polishing; randomly distributed Si nanowires (e) embedded into glue and sectioned by polishing (f).

Figures 2e and 2f illustrate that free-standing silicon nanowires can also be cross-sectioned for SSRM analysis. For this, the frontside of the nanowire sample is glued against a glass slide. It is important to keep the gap in between the two samples as small as possible to avoid extensive smear-out effects during polishing and to reduce nanowire breakage during polishing as much as possible.

The cross-sectioned nanowire sample is inspected by SEM and the location of the cross-sectioned nanowires to be measured in SSRM is marked in such a way that the mark can be seen in the optical microscope of the AFM system. Note that marking is a key step of the procedure; the challenge is to locate a specific nanowire cross-section on a centimeter long sample. Suitable marking is achieved in our experiments in a nanoprobng system by locally scratching a mark using a sharp diamond tip (figure 3a and 3b) or by locally depositing pieces of graphite from a sharpened pencil-lead tip (figure 3c). A focused ion beam (FIB) can be used as well.

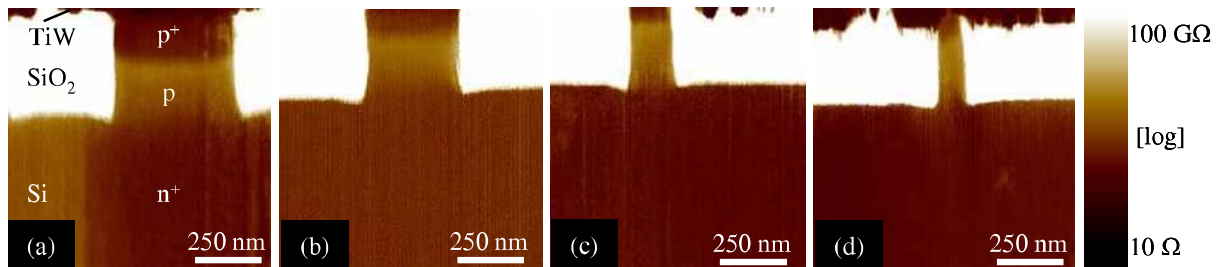
For making electrical contact to the nanowire sample, a copper wire is attached to the bulk silicon using indium gallium eutectic encapsulated by silver conductive glue. For nanowires with incorporated p-n junctions, a thin metal layer of 5 nm TiW is deposited on top of the nanowire sample before the cleaving step. Note that thick metal layers affect cleaving and polishing and show also smear-out effects in SSRM measurements.



**Figure 3.** Suitable marking of the location of the nanowire cross-section is achieved by putting an optically visible mark in close proximity using a diamond tip (a) and scratching (b) or by locally depositing some graphite using a sharpened pencil-lead tip (c).

### SSRM OF SI NANOWIRES

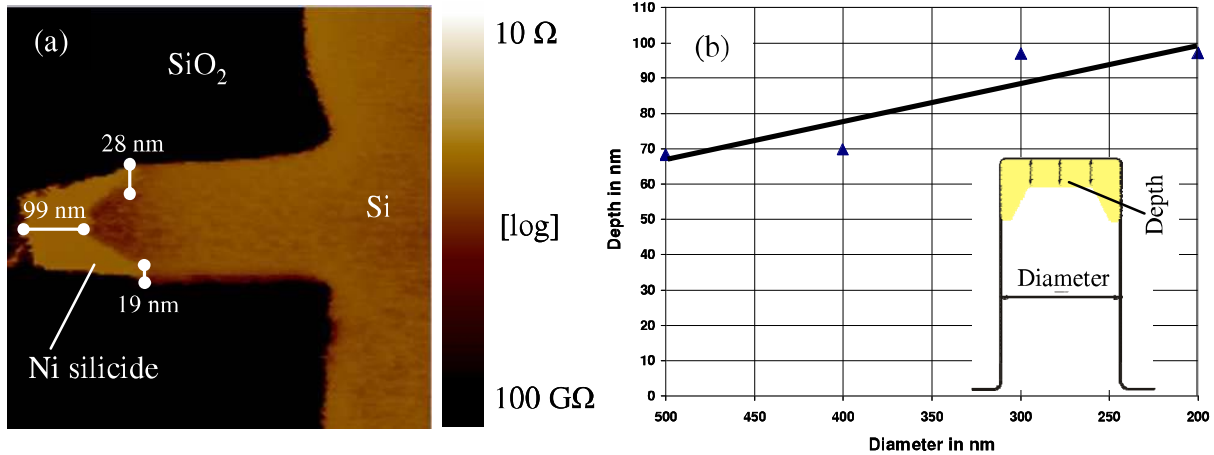
Figure 4 shows etched Si nanowires with a length of 400 nm and diameters ranging from 500 to 100 nm which are characterized by SSRM. The nanowires are embedded into  $\text{SiO}_2$  and have an  $n^+$  bottom region, followed by a p-type nanowire region and a  $p^+$  implanted top region. They are fabricated by a procedure as described elsewhere [10]. In short, the nanowire stack is first grown by silicon wafer epitaxy and then individual nanowires are formed by reactive ion etching (RIE) followed by high-density-plasma (HDP)  $\text{SiO}_2$  deposition, chemical-mechanical polishing (CMP) and implantation. The white color shows non-conductive regions (high resistance) and dark colors represent more conductive regions (low resistance). Note that the differently doped regions of the nanowires can be clearly identified in SSRM which is not possible by other techniques (e.g. SEM or TEM inspection). The SSRM analysis shows also that the nanowires have been etched 10 nm into the  $n^+$  substrate during the RIE step. Note the small notch of about 15 nm in depth around the nanowire base which is typical for nanowires made by RIE. The implanted  $p^+$  region extends 92 nm into the nanowire. The SSRM images illustrate that the developed procedure works for a wide range of nanowire diameters.



**Figure 4.** SSRM of etched Si nanowires with diameters of 500 (a), 300 (b), 200 (c), and 100 nm (d) with  $n^+$  bottom region, n-type nanowire region and boron implanted top region.

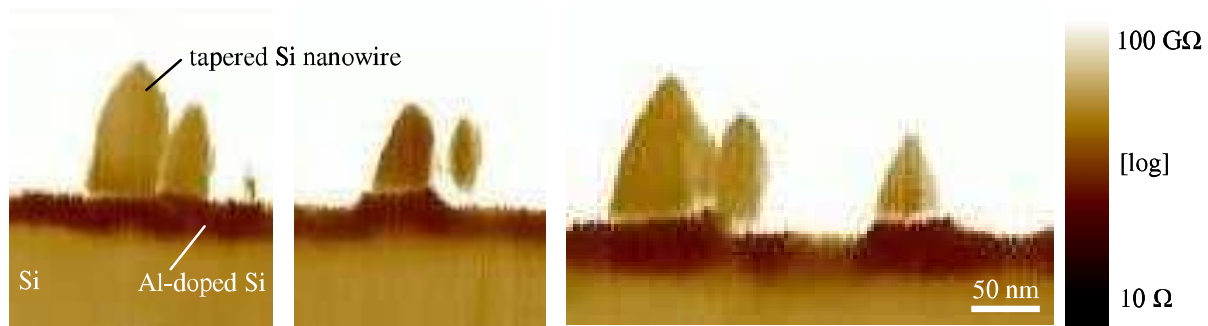
Figure 5 shows an SSRM image of a 200 nm diameter n-type nanowire on p-type substrate with nickel silicide top. These nanowires are made as described above whereby the implantation step is replaced by a nickel silicidation step. Due to an opposite applied bias voltage compared to figure 4, the image contrast is reversed. Hence the  $\text{SiO}_2$  is seen as a black region whereas the nickel silicide is seen as a bright region. Note that the shape and size of the nickel silicide region can be imaged with nanometer resolution despite the limited contrast of one order of magnitude between silicon and silicide for these particular nanowire structures. Our measurements show that for nanowires with diameters from 500 to 200 nm, the silicidation depth

is gradually increasing from 70 nm to 100 nm (see figure 5b). This is expected as with decreasing nanowire diameter, there is an increasing contribution from the nanowire side-wall silicidation. The silicide regions on the upper side-walls of the nanowires originate from exposure of these regions during silicidation.



**Figure 5.** SSRM of 200 nm diameter Si nanowire with Ni silicide top (a); study of silicided Si nanowires of different diameters showing that the silicidation depth is inversional proportional to the diameter and must be taken into account for proper contact engineering.

Figure 6 is an example where SSRM is applied to epitaxially grown nanowires which are fabricated by the vapor-solid-solid (VSS) mechanism using aluminum catalyst (detailed description in reference [5]). In short, aluminum nanoparticles are formed on a (111)-silicon substrate by an evaporation and subsequent annealing step. Tapered silicon nanowires are then grown by ultra-high vacuum chemical vapor deposition (UHV-CVD) using silane diluted to 5% in argon at about 500°C. The nanowire length on the sample ranges from 50 to 500 nm and the diameter is on average about 50 nm. The tilted-view SEM image shown in figure 2e illustrates that the nanowires have a tapered shape, are randomly distributed on the surface and are not surrounded by supporting SiO<sub>2</sub>. Therefore polishing is used for cross-sectioning the nanowires. Figure 2f shows the sample after polishing. As a consequence, the RMS roughness of the cross-sections is slightly higher (typically 0.2-0.3 nm for polishing versus 0.1-0.2 nm for cleaving) and the signal to noise ratio in the SSRM resistance maps is lower. The SSRM image in figure 6 shows three parts which belong to different areas of the same cross-section. The white color indicates a very high resistance; hence the glue is shown in white color. The silicon nanowires have a diameter of about 50 nm. The tapered shape of the nanowires is clearly observed in the SSRM images. Furthermore, a high conductive region of 30 nm in thickness is visible on the top of the silicon substrate. This results from the doping of the silicon surface by diffusion of the aluminium layer into the silicon during the first annealing step. Furthermore, it is observed that the nanowires are in most cases slightly more conductive than the substrate. This is attributed to an Al-doping of the nanowire caused by the Si-Al alloy particle on top of the wire during the growth. Note also the presence of a 3-5 nm wide non-conductive region on the nanowire base which illustrates the high-resolution capability of SSRM. Its origin is not completely understood yet; it might be related to a non-conductive interfacial layer or partial nanowire damaging during polishing.



**Figure 6.** SSRM of epitaxially grown Si nanowires using an Al catalyst and having a tapered shape. A 30 nm thick doped region on the substrate surface is observed caused by diffusion of Al into Si during annealing. The Si nanowires seem also to be doped by the Al catalyst.

## CONCLUSIONS

Silicon nanowires can be characterized by SSRM with a high spatial electrical resolution of around 1 nm. This allows to analyze doped and silicided regions of nanowires and to give important feedback for process optimization. Nanowire cleaving gives a lower surface roughness and is therefore the preferred sectioning method. Nanowire polishing must be used when thick metal layers are involved. For obtaining high-quality cross-sections with a low roughness, the nanowires should be surrounded by a protective coating. We are currently working on quantifying the carrier profiles (requires parallel measurements on doping calibration structures with the same unchanged tip) and to measure also other materials and hetero junctions.

## ACKNOWLEDGMENTS

The authors thank IMEC's Nano program for sample supply and acknowledge the partial support by EU project NODE 015783. Andreas Schulze thanks the Institute for the Promotion of Innovation through Science and Technology in Flanders (IWT) for his Ph.D. fellowship.

## REFERENCES

1. A.S. Verhulst, W.G. Vandenberghe, K. Maex, S. De Gendt, M.M. Heyns, and G. Groeseneken, *IEEE Electron Device Letters* **29**, 1398 (2008).
2. J. Westwater, D. P. Gosain, S. Tomiya, S. Usui, and H. Ruda, *J. Vac. Sci. Technol. B* **15**, 554 (1997).
3. Y. Cui, and C.M. Lieber, *Science* **291**, 851 (2001).
4. V. Schmidt, S. Senz, and U. Gösele, *Nano Lett.* **5**, 931 (2005).
5. Y. Wang, V. Schmidt, S. Senz, and U. Gösele, *Nature Nanotechnology* **1**, 186 (2006).
6. P. De Wolf, J. Snauwaert, T. Clarysse, W. Vandervorst, and L. Hellemans, *Appl. Phys. Lett.* **66**, 1530 (1995).
7. P. Eyben, W. Vandervorst, D. Alvarez, M. Xu, and M. Fouchier, in: *Scanning Probe Microscopy*, edited by S. Kalinin and A. Gruverman, (Springer, 2007), p. 31.
8. T. Hantschel, P. Niedermann, T. Trenkler, and W. Vandervorst, *Appl. Phys. Lett.* **76**, 1603 (2000).
9. T. Hantschel, C. Demeulemeester, P. Eyben, V. Schulz, O. Richard, H. Bender, and W. Vandervorst, *Phys. Status Solidi A*, submitted for publication.
10. P. Agarwal, M.N. Vijayaraghavan, F. Neuilly, E. Hijzen, and G.A.M. Hurkx, *Nano Lett.* **7**, 896 (2007).